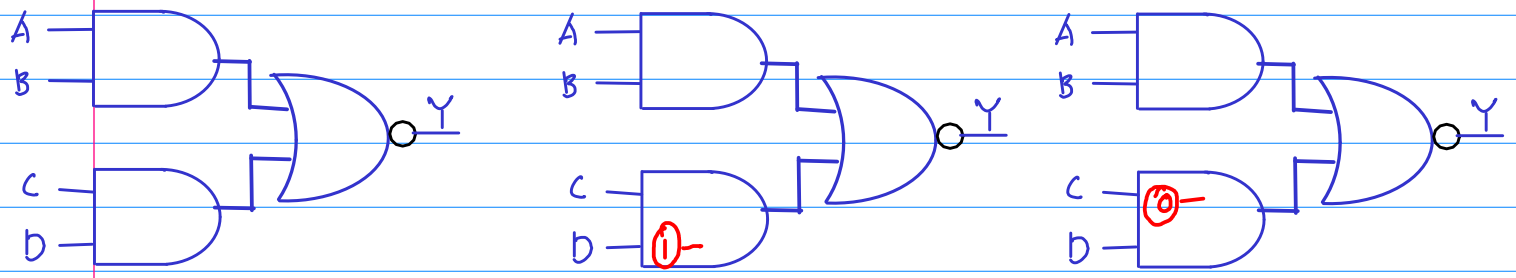
SOC HW #4

20160412

(I) Test

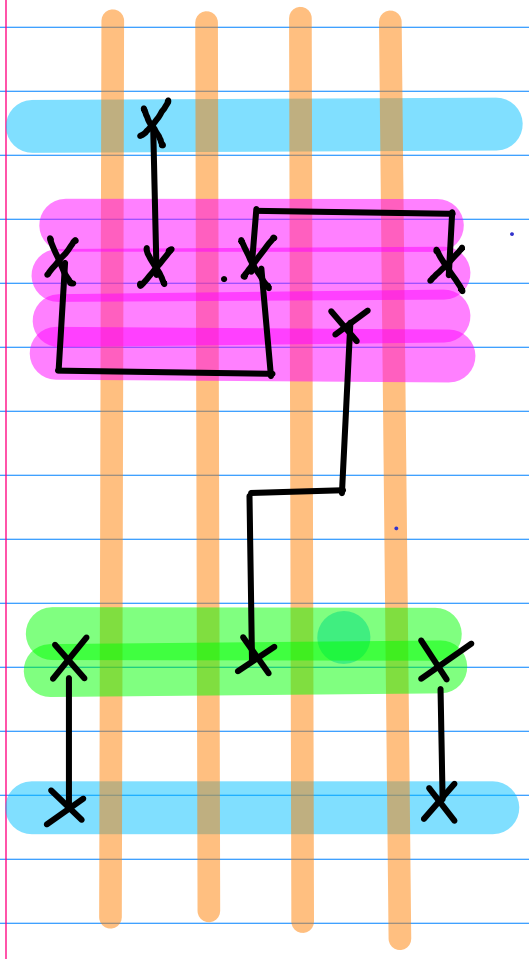
D: SA1

C: SA0

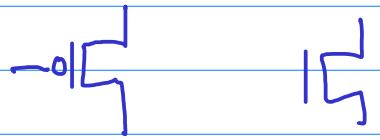


	A	B	C	D	(a) Normal Y	(b) SA1 Y	(c) SA0 Y
0	0	0	0	0			
1	0	0	0	1			
2	0	0	1	0			
3	0	0	1	1			
4	0	1	0	0			
5	0	1	0	1			
6	0	1	1	0			
7	0	1	1	1			
8	1	0	0	0			
9	1	0	0	1			
10	1	0	1	0			
11	1	0	1	1			
12	1	1	0	0			
13	1	1	0	1			
14	1	1	1	0			
15	1	1	1	1			

(d) stick diagram



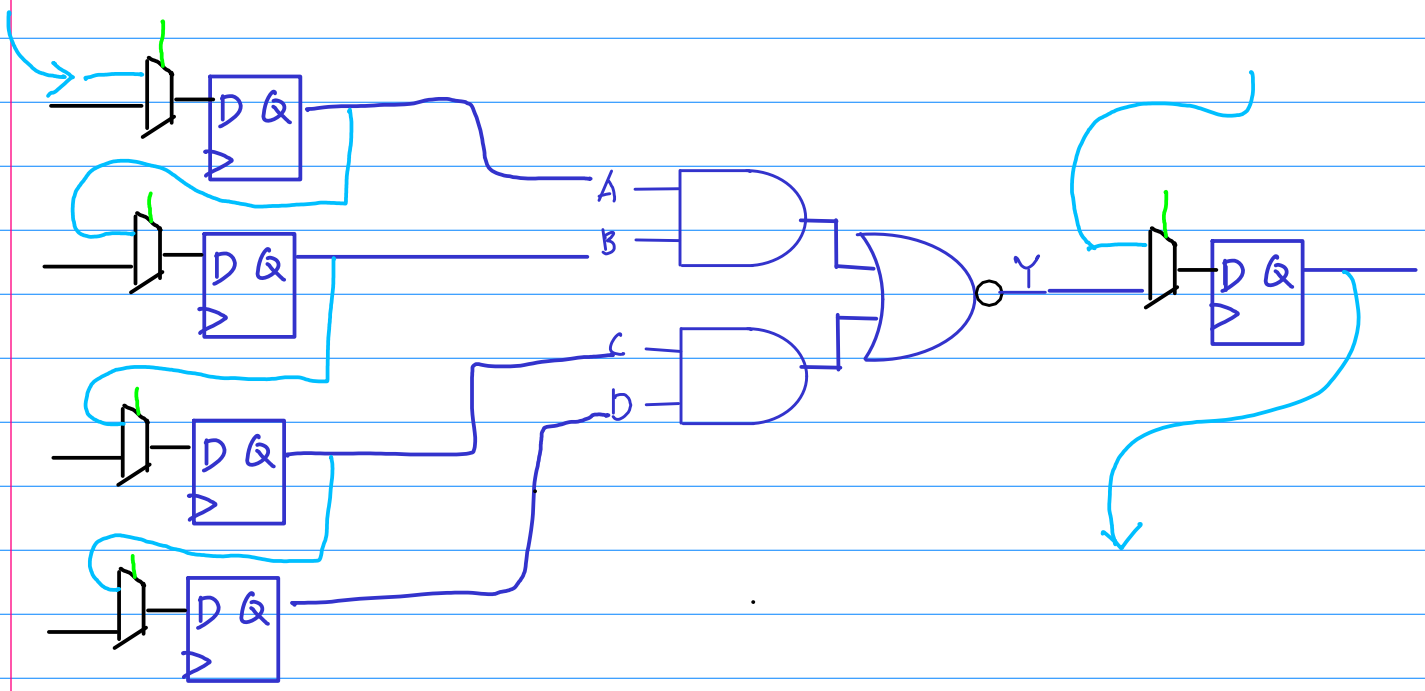
① draw nMOS PDN
pMOS PDN



② SA1 fault at "D" input
explain

③ SA0 fault at "C" input
explain

(e)



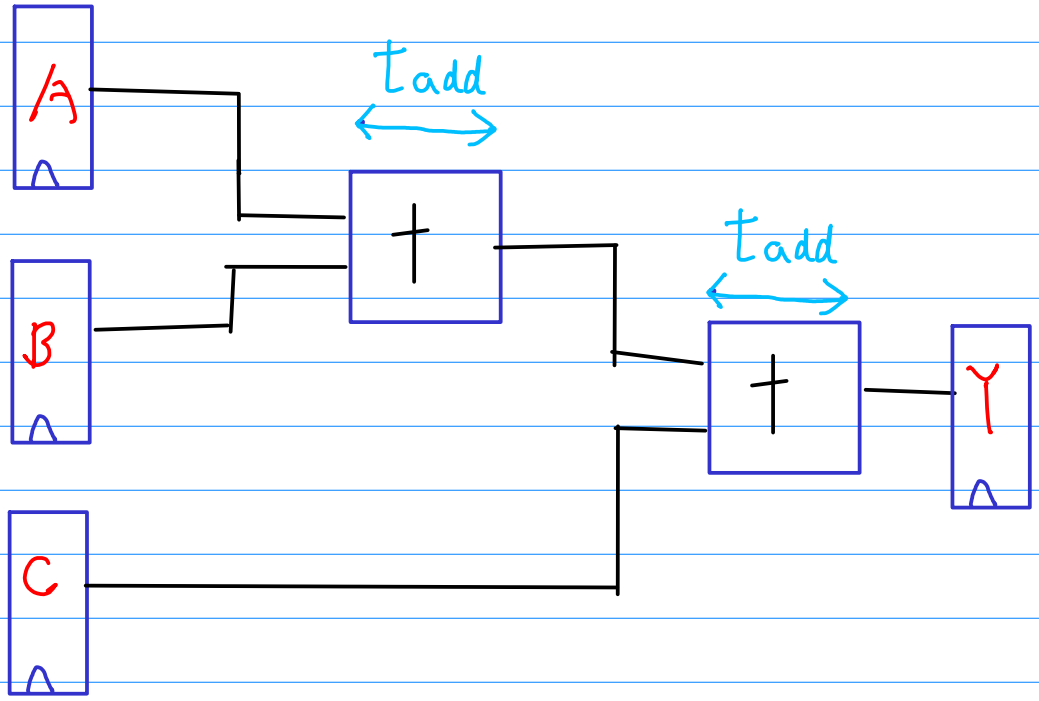
Scan cell을 이용해 SA1과 SA0를
detect하는 방법을 간단히 설명하시오

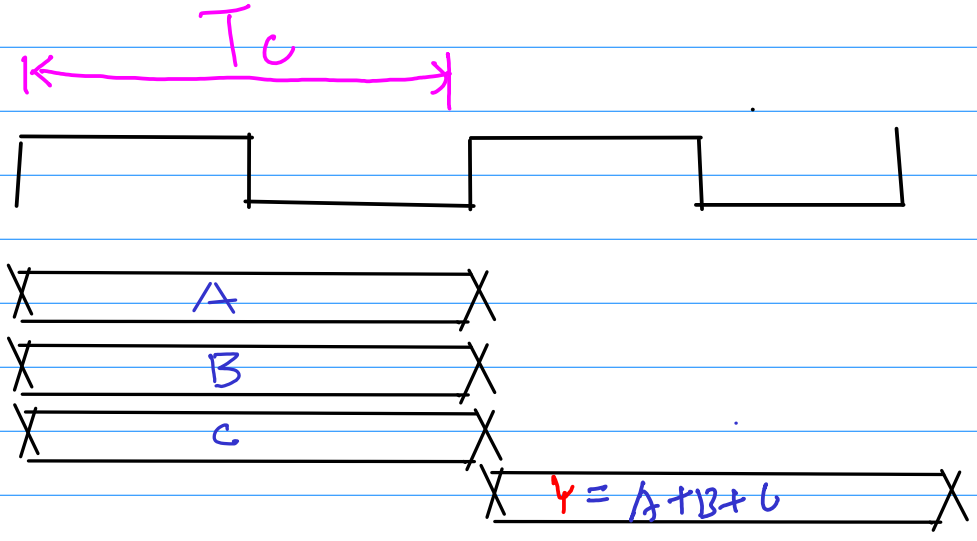
(f) controllability를 위의 값을 사용해 설명하시오

(g) observability " " " "

Ⅱ Pipeline

Adding 3 8-bit number $A+B+C=Y$

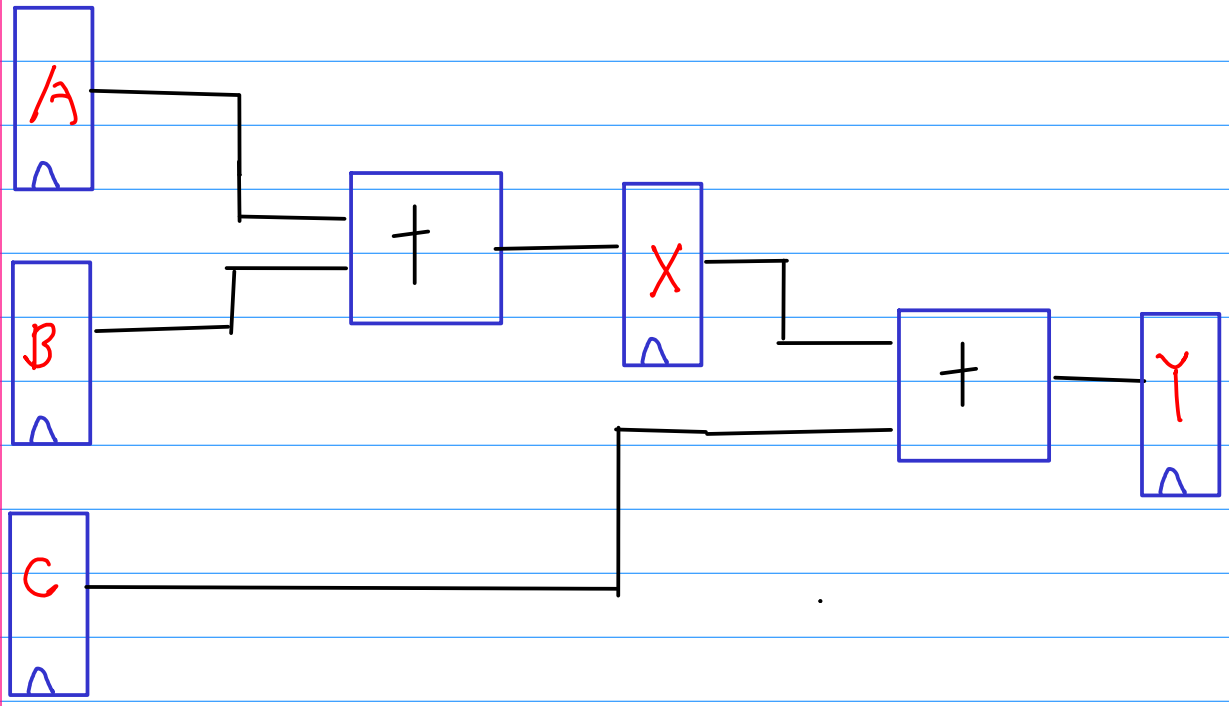


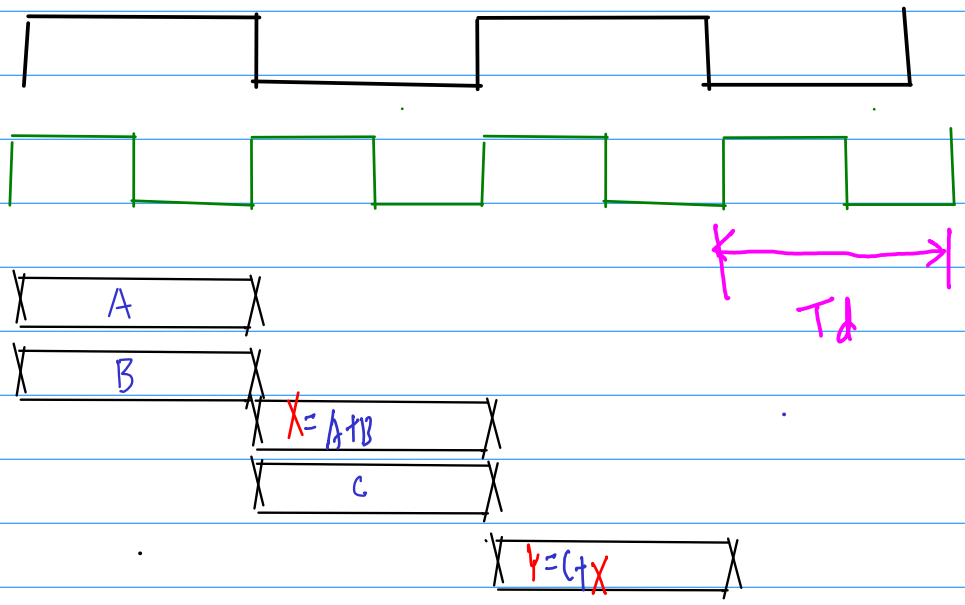


① Tc ≥ ?

② $A_1+B_1+C_1$
$A_2+B_2+C_2$
$A_3+B_3+C_3$
⋮

Timing Diagram





③ $T_d \geq$?

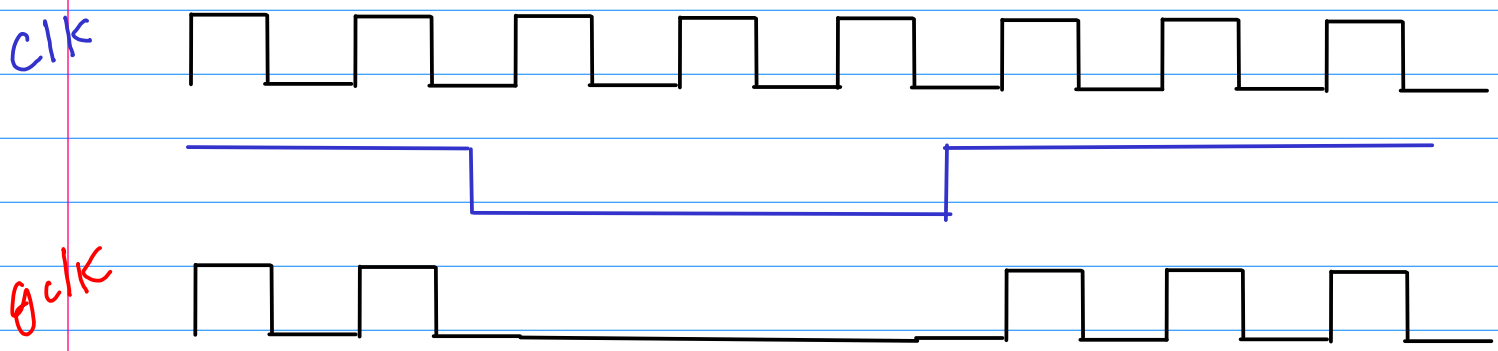
④ $A_1 + B_1 + C_1$
$A_2 + B_2 + C_2$
$A_3 + B_3 + C_3$
⋮

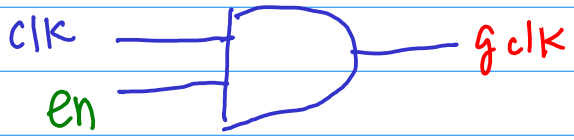
Timing Diagram

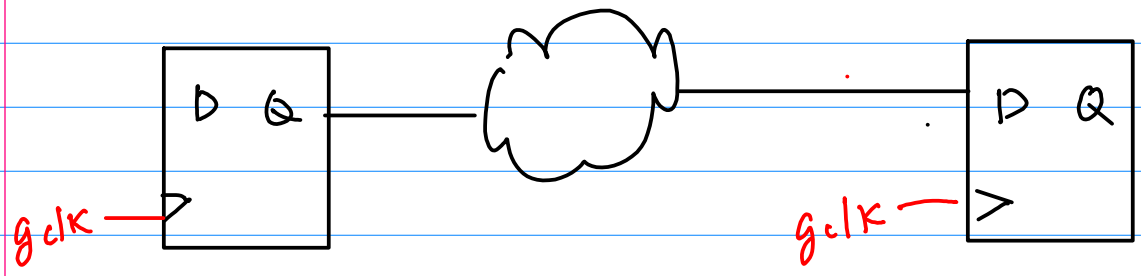
(5) Throughput ?

(6) Latency ?

Ⅲ gated clock







✡ gclk를 사용하면 왜 power가 감소되는가?