

SOC HW #4

20160412

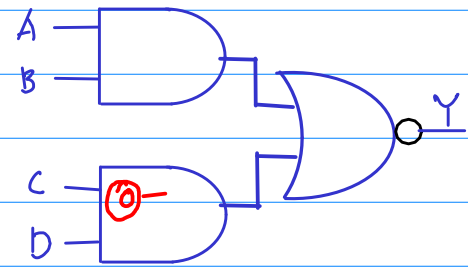
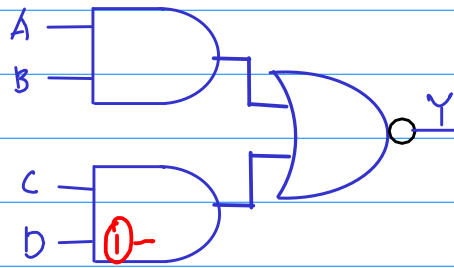
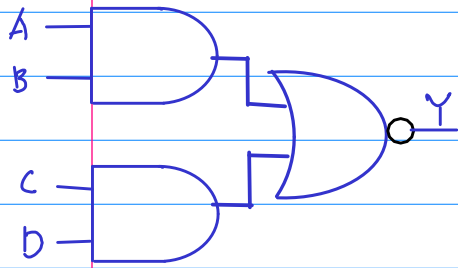
Copyright (c) 2016 Young W. Lim.

Permission is granted to copy, distribute and/or modify this document under the terms of the GNU Free Documentation License, Version 1.2 or any later version published by the Free Software Foundation; with no Invariant Sections, no Front-Cover Texts, and no Back-Cover Texts. A copy of the license is included in the section entitled "GNU Free Documentation License".

I Test

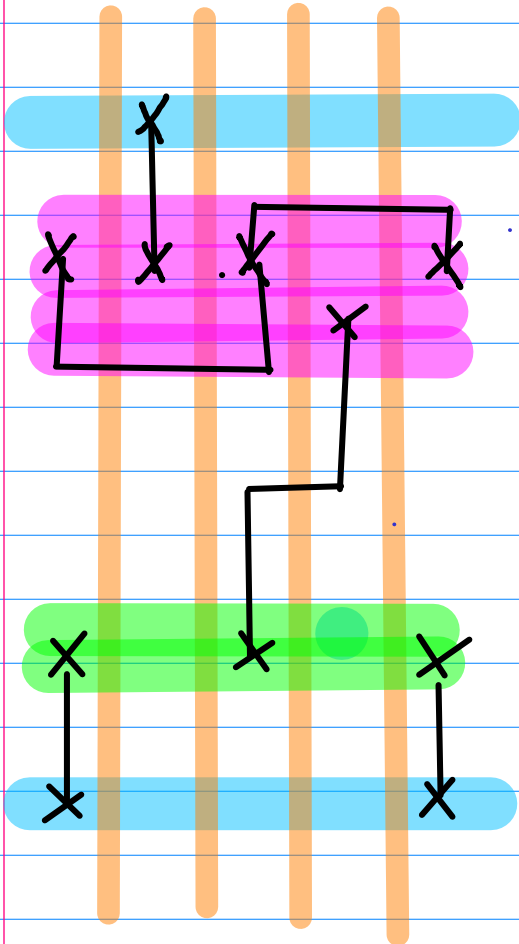
D: SA1

C: SA0

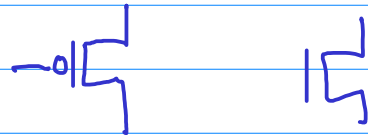


	A	B	C	D	(a) Normal Y	(b) SA1 Y	(c) SA0 Y
0	0	0	0	0			
1	0	0	0	1			
2	0	0	1	0			
3	0	0	1	1			
4	0	1	0	0			
5	0	1	0	1			
6	0	1	1	0			
7	0	1	1	1			
8	1	0	0	0			
9	1	0	0	1			
10	1	0	1	0			
11	1	0	1	1			
12	1	1	0	0			
13	1	1	0	1			
14	1	1	1	0			
15	1	1	1	1			

(d) stick diagram



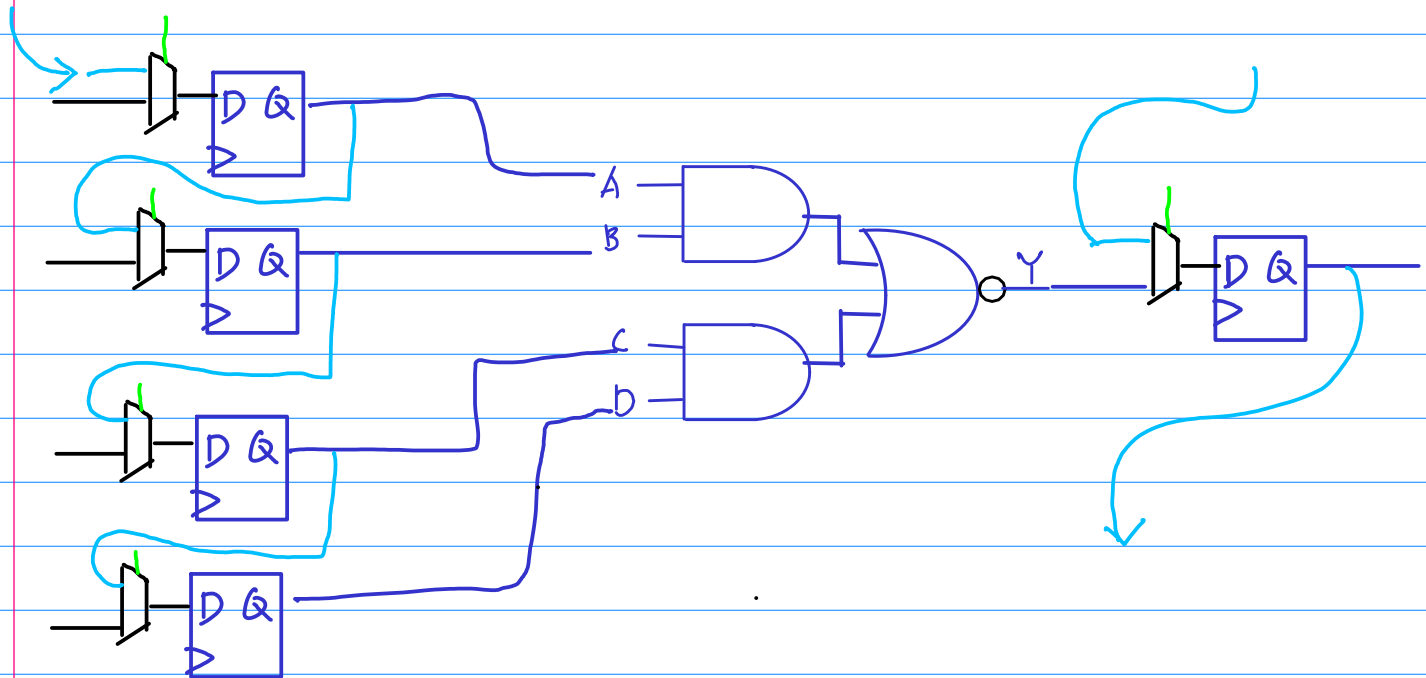
① draw nMOS PDN
pMOS PDN



② SA1 fault at "D" input
explain

③ SA0 fault at "C" input
explain

(e)



Scan cell을 이용하여 SA1과 SA0를
detect하는 방법을 간단히 설명하시오

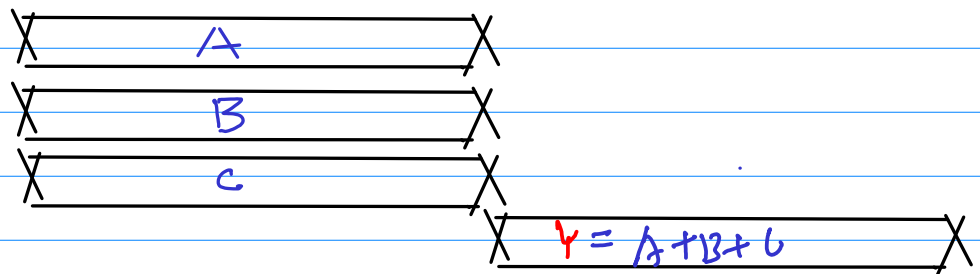
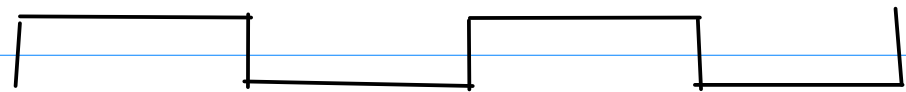
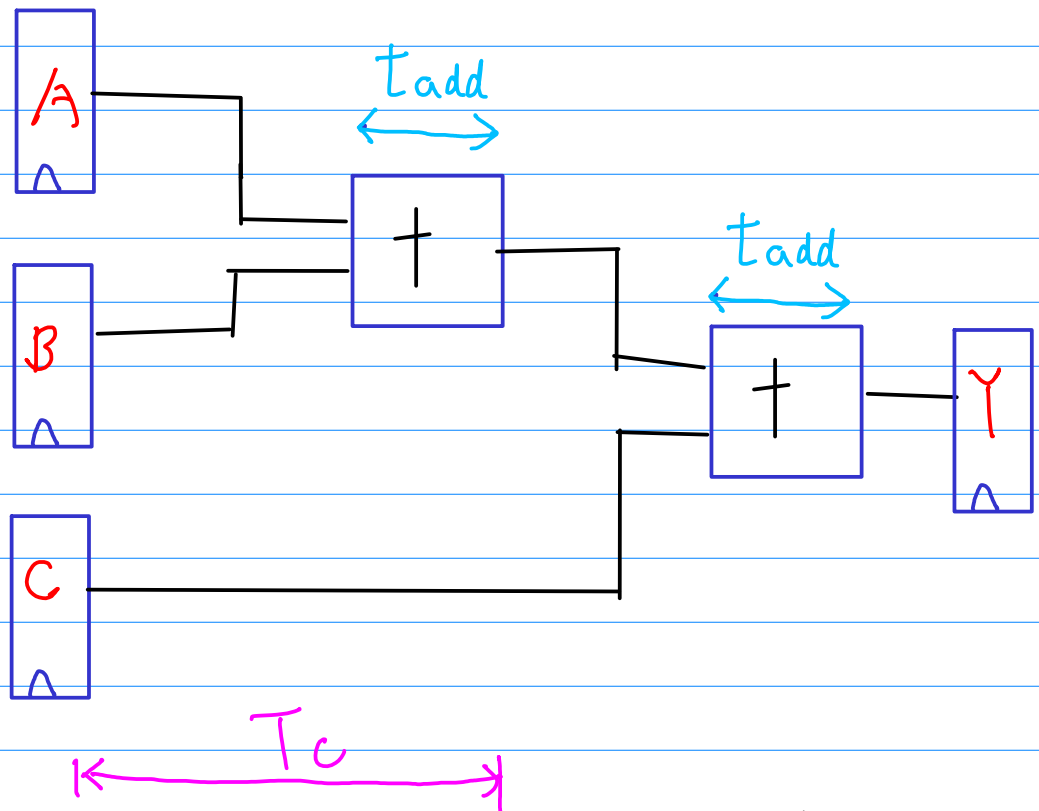
(f) controllability를 위의 그림을 사용하여 설명하시오

(g) observability " " " " "

II

Pipeline

Adding 3 8-bit numbers $A+B+C=Y$

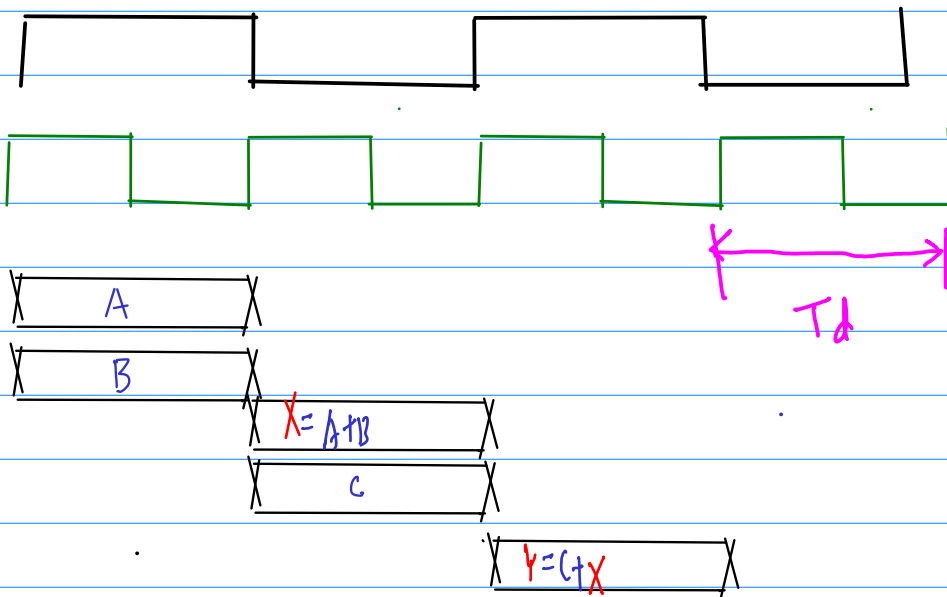
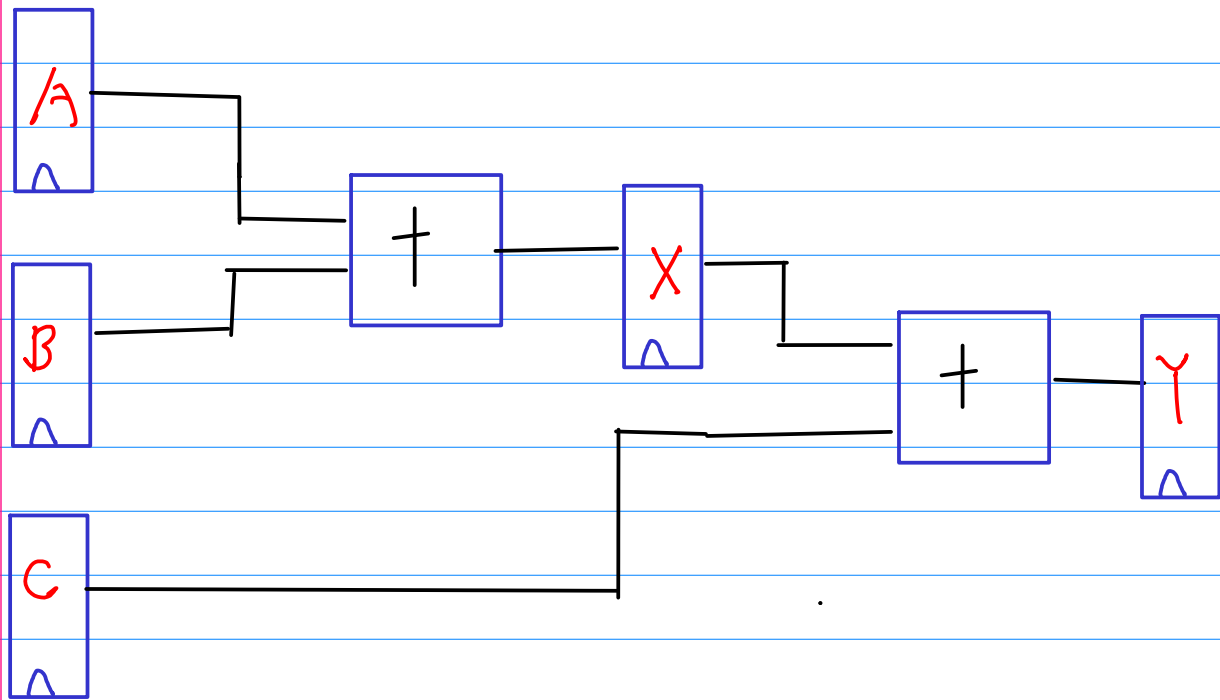


① $T_c \geq \boxed{?}$

②

$$\begin{aligned} &A_1 + B_1 + C_1 \\ &A_2 + B_2 + C_2 \\ &A_3 + B_3 + C_3 \\ &\vdots \end{aligned}$$

) Timing
Diagram



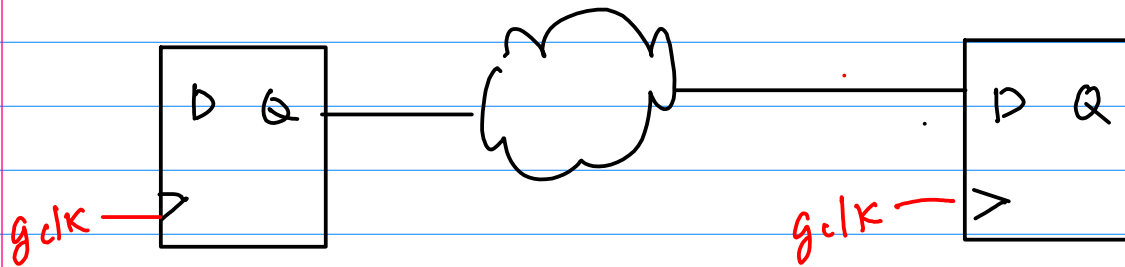
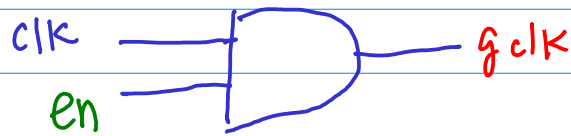
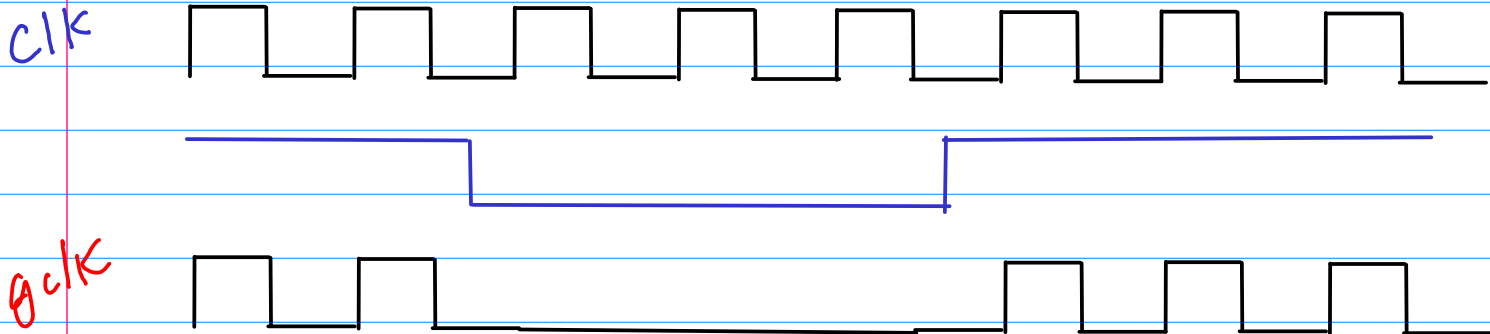
③ $T_d \geq \boxed{?}$

④
$$\begin{matrix} A_1 + B_1 + C_1 \\ A_2 + B_2 + C_2 \\ A_3 + B_3 + C_3 \\ \vdots \end{matrix} \quad \left. \vphantom{\begin{matrix} A_1 + B_1 + C_1 \\ A_2 + B_2 + C_2 \\ A_3 + B_3 + C_3 \\ \vdots \end{matrix}} \right\} \begin{matrix} \text{Timing} \\ \text{Diagram} \end{matrix}$$

(5) Throughput ?

(6) Latency ?

III gated clock



★ gclk를 사용하면 왜 power가 감소되는가?